Electronic Version
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Claims

[c1] 1. A method of improving manufacturing productivity of an integrated circuit, comprising:
(a) generating a set of physical design rules,
(b) assigning a rule scoring equation to each physical design rule of said set of physical design rules;
(c) checking a physical design of said integrated circuit for deviations from each design rule;
(d) computing a score for each physical design rule, using the corresponding rule scoring equation assigned to each physical design rule, for which one or more deviations were found in step (c); and
(e) computing a productivity score for said integrated circuit design based on said scores computed in step (d).

[c2] 2. The method of claim 1, step (b) further including: assigning weighting factors to some or all of said physical design rules, said weighting factor incorporated into the corresponding rule scoring equations.

[c3] 3. The method of claim 1, wherein said set of physical design rules further comprises a set of design efficiency rules and a set of yield limiting rules.

[c4] 4. The method of claim 3, wherein said design efficiency rules are rules for the area of an integrated circuit chip utilized by particular mask levels of said physical design.

[c5] 5. The method of claim 3, wherein step (d) includes:
computing a score for each design efficiency rule, using a corresponding rule scoring equation assigned to each design efficiency rule;
computing a score for each yield limiting rule, using a corresponding rule scoring equation assigned to each yield limiting rule, for which one or more deviations were found in step (c); and
wherein said productivity score is a based on said score for each design efficiency rule and based on an integrated circuit design area normalized function of scores for each yield limiting rule for which one or more deviations were found in step (c).

[c6] 6. The method of claim 4, wherein said particular mask levels include those areas used for active devices such as field effects transistors, the gates of field effect transistors, bipolar transistors and diodes and passive elements such as resistors, inductors, capacitors and fuses.

[c7] 7. The method of claim 1, further including between steps (c) and (d):
providing a list of all design rule violations for which one

or more deviations were found in step (c).

[c8] 8. The method of claim 7, wherein said set of physical design rules are in Design Rule Checking format and said list of all design rules is generated using Design Rule Checking software.

[c9] 9. The method of claim 1, wherein each said rule scoring equation is a linear, power or Gaussain function of a recommended value and an actual design value used in the physical design.

[c10] 10. The method of claim 1, further including:
(f) modifying said physical design of said integrated circuit based on said score for each physical design rule, said productivity score or both said score for each physical design rule and said productivity score.

[c11] 11. A computer system comprising a processor, an address/data bus coupled to said processor, and a computer-readable memory unit coupled to said processor, said memory unit containing instructions that when executed by said processor implement a method for improving manufacturing productivity of an integrated circuit, said method comprising the computer implemented steps of:
(a) generating a set of physical design rules,

(b) assigning a rule scoring equation to each physical design rule of said set of physical design rules;
(c) checking a physical design of said integrated circuit for deviations from each design rule;
(d) computing a score for each physical design rule, using the corresponding rule scoring equation assigned to each physical design rule, for which one or more deviations were found in step (c); and
(e) computing a productivity score for said integrated circuit design based scores computed in step (d).

[c12] 12. The system of claim 11, step (b) further including: assigning weighting factors to some or all of said physical design rules, said weighting factor incorporated into the corresponding rule scoring equations.

[c13] 13. The system of claim 11, wherein said set of physical design rules further comprises a set of design efficiency rules and a set of yield limiting rules.

[c14] 14. The system of claim 13, wherein said design efficiency rules are rules for the area of an integrated circuit chip utilized by particular mask levels of said physical design.

[c15] 15. The system of claim 13, wherein step (d) includes: computing a score for each design efficiency rule, using

a corresponding rule scoring equation assigned to each design efficiency rule;

computing a score for each yield limiting rule, using a corresponding rule scoring equation assigned to each yield limiting rule, for which one or more deviations were found in step (c); and

wherein said productivity score is a based on said score for each design efficiency rule and based on an integrated circuit design area normalized function of scores for each yield limiting rule for which one or more deviations were found in step (c).

[c16] 16. The system of claim 14, wherein said particular mask levels include those areas used for active devices such as field effects transistors, the gates of field effect transistors, bipolar transistors and diodes and passive elements such as resistors, inductors, capacitors and fuses.

[c17] 17. The system of claim 11, further including between steps (c) and (d):

providing a list of all design rule violations for which one or more deviations were found in step (c).

[c18] 18. The system of claim 17, wherein said set of physical design rules are in Design Rule Checking format and said list of all design rules is generated using Design Rule Checking software.

[c19] 19. The system of claim 11, wherein each said rule scoring equation is a linear, power or Gaussain function of a recommended value and an actual design value used in the physical design.

[c20] 20. The system of claim 1, further including:
(f) modifying said physical design of said integrated circuit based on said score for each physical design rule, said productivity score or both said score for each physical design rule and said productivity score.